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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/575,244	04/10/2006	Einar Nygard	1268-260	7106
22429 7590 11/15/2007 LOWE HAUPTMAN HAM & BERNER, LLP 1700 DIAGONAL ROAD SUITE 300 ALEXANDRIA, VA 22314			EXAMINER SOHN, SEUNG C	
			ART UNIT 2878	PAPER NUMBER
			MAIL DATE 11/15/2007	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

Application No.

10/575,244

Applicant(s)

NYGARD, EINAR

Examiner

SEUNG C. SOHN

Art Unit

2878

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3-8 and 10-12 is/are rejected.
- 7) ☒ Claim(s) 2,9,13 and 14 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 20060410.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. ***Claims 6-7 and 12 are rejected under 35 U.S.C. 112, second paragraph***, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

**Regarding claim 6**, it is not clear what the claimed scope is since the sentence is not completed. Clarification is required.

**Claims 7 and 12** provide for the use of manufacturing methods of claim 1 and device of claim 8, respectively, but, since the claims do not set forth any steps involved in the method/process, it is unclear what method/process applicant is intending to encompass. A claim is indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

**Claims 7 and 12** are rejected under 35 U.S.C. 101 because the claimed recitation of a use, without setting forth any steps involved in the process, results in an improper definition of a process, i.e., results in a claim which is not a proper process claim under 35 U.S.C. 101. See for example *Ex parte Dunki*, 153 USPQ 678 (Bd.App. 1967) and *Clinical Products, Ltd. v. Brenner*, 255 F. Supp. 131, 149 USPQ 475 (D.D.C. 1966).

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. ***Claims 1, 8 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Tewksbury et al ("Cointegration of optoelectronics and submicron CMOS," Wafer Scale Information, 1993 Proceedings, Fifth Annual IEEE International Conference on San Francisco, CA USA; Jan. 20, 1993; Pages 358-367).***

Regarding claim 1, Tewksbury et al. discloses the steps of integrating the electronic processing circuits on a CMOS wafer by stitching a plurality of reticles of at least two different types so as to form an integrated circuit having an array of electronic processing circuits each having a respective sensor input disposed toward a first surface of the wafer and accessible from the first surface via a terminal pad formed near an edge of the integrated circuit such that each terminal pad serves to access multiple sensor inputs via a controller fabricated at an edge of the wafer; and disposing the sensor elements on the first surface of the respective integrated circuits in said detector whereby an exposed surface of the sensor elements forms a common first electrode towards which incident photons are directed, and an opposite unexposed surface thereof forms multiple second electrodes of opposite polarity to the first electrode each in registration with a corresponding sensor input (Figs. 6-9, Pages 363-366).

**Regarding claim 8**, Tewksbury et al. shows in Fig. 6-9 at least one integrated circuit formed by stitching a plurality of reticles of at least two different types and having an array of electronic processing circuits each having a respective sensor input disposed toward a first surface of the wafer and accessible from the first surface via a terminal pad formed near an edge of the integrated circuit such that each terminal pad serves to access multiple sensor inputs via a controller fabricated at an edge of the wafer; and sensor elements disposed on the first surface of the at least one integrated circuit in said detector assembly whereby an exposed surface of the sensor elements forms a common first electrode towards which incident photons are directed, and an opposite unexposed surface thereof forms multiple second electrodes of opposite polarity to the first electrode each in registration with a corresponding sensor input (Figs. 6-9, Pages 363-366).

**Regarding claim 11**, Tewksbury et al. discloses that the sensor elements include monolithically integrated crystalline sensors mounted on the first surface of the wafer in registration with respective sensor inputs.

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**6. Claims 3-5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tewksbury et al ("Cointegration of optoelectronics and submicron CMOS," Wafer Scale Information, 1993 Proceedings, Fifth Annual IEEE International Conference on San Francisco, CA USA; Jan. 20, 1993; Pages 358-367) in view of Cheung (US Patent No. 6,416,218 B1).**

Regarding claims 3-5 and 10, Tewksbury et al. discloses the steps of claim 1 and the device of claim 8, but does not disclose the step of disposing the sensor elements includes growing on the first surface of the wafer amorphous or polycrystalline sensor material that is capable of detecting incident photons directly and the step of mounting the detector assembly on a PCB prior to disposing the sensor elements. Cheung discloses the step of disposing the sensor elements includes growing on the first surface of the wafer amorphous or polycrystalline sensor material that is capable of detecting incident photons directly and the step of mounting the detector assembly on a PCB prior to disposing the sensor elements (Col. 5, line 58 – Col. 8, line 20). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the invention of Tewksbury et al. with the step of growing on the first surface of the wafer amorphous or polycrystalline sensor material that is capable of detecting incident photons directly and the step of mounting the detector assembly on a PCB prior to disposing the sensor elements, as taught by Cheung, in order to follow standard procedures to make a wafer.

***Allowable Subject Matter***

7. **Claims 2, 9 and 13-14** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

**Claims 2, 9 and 13-14** are not disclosed or made obvious by the prior art of record, specifically in combination with the limitation of "a very large area rectangular CMOS wafer having a major edge and a minor edge, the major having a dimension (L) that is substantially half of a width of the detector and having at least one array of electronic processing circuits each electronic processing circuit having a respective sensor input disposed toward a first surface of the wafer and accessible from the first surface via a terminal pad formed towards a minor edge of the sensor array, such that each terminal pad serves to access multiple sensor inputs via a controller fabricated at an edge of the wafer".

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SEUNG C. SOHN whose telephone number is 571-272-4123. The examiner can normally be reached on M-TH, 8 AM -7 PM.

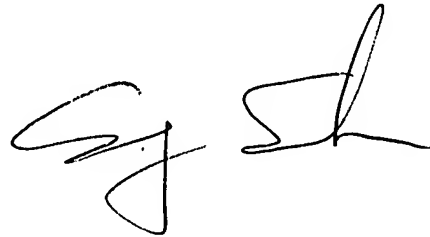
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, GEORGIA Y. EPPS can be reached on 571-272-2328. The fax phone

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number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

A handwritten signature in black ink, appearing to read 'Sj Sh', is positioned above the printed name of the examiner.

SEUNG C SOHN  
Examiner  
Art Unit 2878